# LESSON PLAN

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| Name of the Faculty | | Sunil Kaushik |
| Discipline | | B.Tech. |
| semester | | IV Sem. |
| subject | | Computer Architecture and Organization |
| Paper Code | | PCC-CSE-211 |
| Lesson plan duration | | From 28th Jan 2023 to May 2023 |
| work load lecture per week(in hours) | | 3 lectures |
| Week | Theory | |
| | Lecture Day | Topic (including assignment/test) |
| 1st | 1 | Boolean algebra and Logic gates, Combinational logic blocks |
| | 2 | Sequential logic blocks |
| | 3 | Sequential logic blocks |
| 2nd | 4 | Sequential logic blocks |
| | 5 | Store program control concept |
| | 6 | Flynn's classification of computers |
| 3rd | 7 | Multilevel viewpoint of a machine |
| | 8 | Digital logic, micro architecture |
| | 9 | ISA, operating systems |
| 4th | 10 | High level language; structured organization |
| | 11 | CPU, caches, main memory |
| | 12 | Secondary memory units & I/O; |
| 5th | 13 | Performance metrics |
| | 14 | MIPS, MFLOPS |
| | 15 | Instruction set based classification of processors |
| 6th | 16 | Instruction set based classification of processors |
| | 17 | Addressing modes: register, immediate, direct, indirect, indexed |
| | 18 | Operations in the instruction set |
| 7th | 19 | Arithmetic and Logical, Data Transfer, Control Flow |
| | 20 | Instruction set formats |
| | 21 | Language of the machine: 8086 |
| 8th | 22 | Simulation using MSAM. |
| | 23 | CPU Architecture types |
| | 24 | CPU Architecture types |
| 9th | 25 | CPU Architecture types |
| | 26 | Detailed data path of a typical register based CPU |
| | 27 | Fetch-Decode-Execute cycle |
| 10 th | 28 | Micro instruction sequencing, implementation of control unit |
| | 29 | Enhancing performance with pipelining |
| | 30 | The need for a memory hierarchy |
| 11 th | 31 | Locality of reference principle, Memory hierarchy in practice |
| | 32 | Cache, main memory and secondary memory, Memory parameters access/ cycle time, cost per bit |

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| | 33 | Main memory (Semiconductor RAM & ROM organization, memory expansion, Static & dynamic memory types |
| 12 th | 34 | Cache memory (Associative & direct mapped cache organizations |
| | 35 | Goals of parallelism (Exploitation of concurrency, throughput enhancement); |
| | 36 | Amdahl's law |
| 13 th | 37 | Instruction level parallelism (pipelining, super scaling –basic features |
| | 38 | Processor level parallelism (Multiprocessor systems overview). |
| | 39 | Instruction codes, computer register, |
| 14 th | 40 | Computer instructions, timing and control |
| | 41 | Instruction cycle |
| | 42 | Iype of instructions, memory reference,register reference |
| 15 th | 43 | I/O reference, Basics of Logic Design, accumulator logic, Control memory |
| | 44 | Address sequencing, micro-instruction format |
| | 45 | Micro-program sequencer, Stack Organization |
| 16 th | 46 | Instruction Formats, Types of interrupts; Memory Hierarchy |